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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,480	06/14/2001	Hsiang-Lan Lung	15313.1	8120

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EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	9

DATE MAILED: 05/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/882,480	Applicant(s) LUNG, HSIANG-LAN	
	Examiner Marcos D. Pizarro-Crespo	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *11-21 and 26-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-31* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Attorney's Docket Number: 15313.1
Filing Date: 6/14/2001
Claimed Foreign Priority Date: none
Applicant(s): Lung
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 8 filed on 3/25/2003.

Acknowledgment

1. The amendment in paper no. 8, filed on 3/25/2003, in response to the Office action in paper no. 6, mailed on 9/25/2002, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-31.

Product-by-Process Claims

2. Initially, and with respect to claims 5 and 6, note that "product by process" claims are directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein that makes it clear that it is the final product *per se* which must be determined in "product by process" claims, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

> even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re*

Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that Applicant has burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6, 22, 23, and 25, are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura (US 5300799).

5. Regarding claim 1, Nakamura shows (see, *e.g.*, fig. 1) all aspects of the instant invention including a single-transistor ferroelectric memory-cell comprising:

- a semiconductor substrate **1** having defined thereon:
  - a first conductive region (*i.e.*, element forming region) of a first conductivity type (*i.e.*, p-type). See, *e.g.*, col.3/ll.60-62.
  - source and drain regions **4, 5, 6** of a second conductivity type (*i.e.*, n-type) defined in the first conductive region
  - a channel region comprising a portion of the first conductive region between the source/drain regions **4, 5,** 6

- a gate oxide layer **7** disposed on the substrate **1** to cover the entirety of the drain, channel, and source regions **4, 5**, 6

➢ a ferroelectric gate unit **FC1** disposed on the gate oxide layer **7** comprising:

- a bottom electrode **10** in electrical communication with the drain region **5, 6**
- a top electrode **12**
- a ferroelectric layer **11** between the bottom **10** and the top **12** electrodes
- a sealing layer **13** disposed on each side of the ferroelectric gate unit **FC1**

➢ an upper conductive layer **14** disposed on the ferroelectric gate unit **FC1** and a portion of the gate oxide layer **7** such that the upper conductive layer **14** and the top electrode **12** of the ferroelectric gate unit **FC1** are in electrical communication (see, *e.g.*, col.5/ll.47-60)

wherein the source region **5** is sized and configured to comprise a portion of said memory cell and an adjacent ferroelectric memory cell.

6. Regarding claim 6, Nakamura shows the source and drain regions of a second conductivity type including As ions implanted therein (col.4/ll.43-45).

7. Regarding claim 22, Nakamura shows (see. *e.g.*, fig. 1) a ferroelectric memory cell comprising:

➢ a ferroelectric gate unit **FC1** comprising:

- a top electrode **12**
- a layer **11** of ferroelectric material
- a bottom electrode **10**

➢ a semiconductor substrate **1** having:

- a drain **5, 6**
- a source **4, 5**
- a channel

➢ a gate oxide **7** substantially covering the drain, source, and channel

➢ means for controlling the polarization of the layer of ferroelectric material (see, *e.g.*, col.5/ll.47-60)

8. Regarding claim 23, Nakamura shows that the means for controlling the polarization of the layer of ferroelectric material comprises an electrical connection between the drain and the bottom electrode of the ferroelectric gate unit.

9. Regarding claim 25, Nakamura shows the memory cell further comprising a lower polysilicon layer deposited between the ferroelectric gate unit and the gate oxide.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Hoshiba (US 5506748).

12. Regarding claim 2, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above). Nakamura (see, *e.g.*, col.5/ll.27), however, differently shows that the upper conductive layer is made out of Al-Si instead of doped polysilicon.

Nonetheless, doped polysilicon and Al-Si are known in the art as equivalent materials (see, *e.g.*, Hoshiba, col.4/ll.36-45). In other words, one skilled in the art would have used any one of these two materials to make Nakamura's upper conductive layer.

Consequently, it would have been obvious at the time of the invention to use either polysilicon or Al-Si to make Nakamura's upper conductive layer, as taught by Hoshiba, since these are equivalent materials for their use in the semiconductor art and selecting any of these known equivalents to make Nakamura's upper conductive layer would be within the level of ordinary skill in the art.

13. Regarding claim 24, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above). In addition, Nakamura shows that an upper conductive layer deposited on top of the ferroelectric gate unit, such that electrical communication is established between the top electrode and the upper conductive layer, may be used to control the polarization of the layer of ferroelectric material (see, *e.g.*, col.5/ll.47-60). See also the comments stated above in paragraph 12 with respect to claim 2, which are considered repeated here.

14. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Krivokapic (US 6100558).

15. Regarding claim 3, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above). Nakamura also shows (see, *e.g.*, fig. 1) the memory cell comprising a plurality of LOCOS isolation fields **2** in the substrate **1**, but fails to show a plurality of shallow isolation trenches (STIs).

Krivokapic (see, *e.g.*, col.5/ll.12-16) teaches that LOCOS isolation fields occupy a great deal of substrate area. STIs, on the other hand, provides for an alternative isolation technique.

It would have been obvious at the time of the invention to substitute Nakamura's LOCOS isolation fields for STIs, as suggested by Krivokapic, to reduce the amount of surface area covered by the LOCOS isolation fields.

16. Claims 4, 7, and 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura.

17. Regarding claim 4, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above). In addition Nakamura shows the memory cell comprising a lower polysilicon layer **8** disposed between the gate oxide layer **7** and the bottom electrode **10**, the lower polysilicon layer **8** doped to a conductive state (see, *e.g.*, fig. 1 and col.4/ll.33-37). Nakamura, however, fails to specify the thickness of the polysilicon layer. Nonetheless, the specific thickness claimed by the applicant, *i.e.*, 500-700 angstroms, absent any criticality, is only considered to be the "optimum" thickness of the layer disclosed by Nakamura that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained as long as a polysilicon layer is used, as already suggested by Nakamura.

18. Regarding claim 7, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above). In addition, Nakamura shows that the bottom **10** and top **12**electrodes may be made of Pt and that the bottom electrode may be 1000 Å thick (see, *e.g.*, col.4/ll.53-64 and col.5/ll.5-11). However, Nakamura fails to specify the thickness of the top electrode. See the comments stated above in paragraph 17 with respect to claim 4 and which are considered repeated here.

19. Regarding claim 8, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above). In addition, Nakamura shows (see, *e.g.*, col.4/ll.64-col.5/ll.5) that the ferroelectric layer may be a $Pb(Zr,Ti)O_3$ layer, which may be about 3000 Å thick, instead of the claimed range of about 800 to 2000 Å. Nonetheless, 2000 Å is close enough to 3000 Å that one of ordinary skill in the art would have expected Nakamura's ferroelectric layer to have the same properties if made having a thickness of 2000 Å. This is supported by the fact that the applicants are claiming the same layer (*i.e.*, a PZT layer), for the same use (*i.e.*, as a dielectric capacitor) and in the same configuration (*i.e.*, in a ferroelectric gate unit of a ferroelectric memory cell), as that of Nakamura's ferroelectric layer.

20. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Jaeger.

21. Regarding claim 5, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above), except that the first conductive region of a first conductivity type includes ions implanted therein, the ions taken from the group consisting of B and BF_2. Nonetheless, Nakamura shows (see, *e.g.*, fig. 1) that the first conductive region is of a

p-type conductivity. According to Jaeger (pp.79/ll.26), boron is the only commonly used p-type dopant.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art that the p-type region of Nakamura should include boron ions, as taught by Jaeger, since boron is the only commonly used p-type dopant.

As to the method step of implanting the ions, this is an intermediate process step that does not affect the structure of the final device. See MPEP § 2113, which discusses the handling of product-by-process claims.

22. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Takenaka (US 6339008).

23. Regarding claim 9, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above). Nakamura, however, shows a PSG sealing layer (see, *e.g.*, col.4/ll.48-52), instead of a Si_3N_4 or an Al_2O_3 layer. Nonetheless, PSG and Si_3N_4 are known in the art as equivalent materials (see, *e.g.*, Takenaka, col.4/ll.5-7). In other words, one skilled in the art would have used any one of these two materials to make Nakamura's sealing layer.

Consequently, it would have been obvious at the time of the invention to use either PSG and Si_3N_4 to make Nakamura's sealing layer, as taught by Takenaka, since these are equivalent materials for their use in the semiconductor art and selecting any of these known equivalents to make Nakamura's sealing layer would be within the level of ordinary skill in the art.

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Schmidt (US 6172392).

25. Regarding claim 10, Nakamura shows most aspects of the instant invention (see paragraphs 5-9 above), but fails to specify a channel length of 0.18 to 0.35 μm.

Schmidt (col.1/ll.16-23), on the other hand, teaches that the semiconductor processing-technology has progressively moved toward defining smaller features, characterized by transistors with a channel length of 0.18 μm. As feature size shrinks, the density of the resulting circuit increases.

Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention that the channel length of the memory cell of Nakamura should have a channel of 0.18 μm, as taught by Schmidt, since channel lengths of 0.18 μm are a characteristic feather of the current semiconductor technology that strives to increase circuit densities.

Response to Arguments

26. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

28. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

29. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is (703) **308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

31. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at (703) 308-**0956**.

32. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/295,314-326,389; 438/3,279; 365/145	5/12/2003
Other Documentation: PLUS Analysis	9/14/2002
Electronic Database(s): EAST (USPAT, EPO, JPO, PGPub)	5/12/2003

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